What is Claimed is:

1. A switch circuit for selectively providing a reference voltage to a logic device, the switch circuit comprising a transmission switch circuit receiving the reference voltage signal at an input thereof and passing the reference voltage signal to an output thereof in response to a first control signal, the first control signal having a logic level determined by a dedicated supply signal, and the dedicated supply signal being different from an input/output supply signal for the logic device.

2. The switch circuit of claim 1 wherein the logic device is operable in accordance with a plurality of input/output standards each having a specified input/output supply signal level, wherein at least one of the plurality of input/output standards is a voltage-referenced standard, and wherein the dedicated supply signal has a voltage level greater than the lowest specified input/output supply signal level for any voltage-referenced standard.

3. The switch circuit of claim 1 wherein the dedicated supply signal has a voltage level of about 2.5 V or greater.

4. The switch circuit of claim 1 wherein the transmission switch circuit comprises a transistor having a control terminal for receiving the first control signal.

5. The switch circuit of claim 4 wherein the transistor is an n-channel metal oxide semiconductor (NMOS) field effect transistor having a gate terminal for receiving the first control signal.

6. The switch circuit of claim 5 wherein a source terminal of the NMOS transistor provides the transmission switch circuit input and a drain terminal of the NMOS transistor provides the transmission switch circuit output.

7. The switch circuit of claim 5 wherein the transmission switch circuit further comprises a p-channel metal oxide semiconductor (PMOS) field effect transistor having a

gate terminal for receiving a second control signal complementary to the first control signal, the PMOS transistor being in parallel with the NMOS transistor, and wherein the transmission switch circuit passes the reference voltage signal to the transmission switch circuit output in response to the first and second control signals.

8. The switch circuit of claim 1 further comprising a first logic level shifting circuit receiving a master control signal at an input thereof, the master control signal having a logic level determined by a first supply signal, the first logic level shifting circuit further receiving the dedicated supply signal and providing the first control signal at an output thereof.

9. The switch circuit of claim 8 further comprising a second logic level shifting circuit receiving the master control signal at an input thereof, the second logic level shifting circuit further receiving the input/output supply signal and providing a second control signal at an output thereof.

10. The switch circuit of claim 8 wherein when the master control signal is at the logic level determined by the first supply signal, the first control signal is at the logic level determined by the dedicated supply signal.

11. The switch circuit of claim 8 wherein the master control signal is provided by a logic core of the logic device and wherein the first supply signal is a core supply signal.

12. The switch circuit of claim 1 wherein the transmission switch circuit comprises first and second n-channel metal oxide semiconductor (NMOS) field effect transistors each having a gate terminal for receiving the first control signal.

13. The switch circuit of claim 12 wherein a source terminal of the first NMOS transistor provides the transmission switch circuit input, a drain terminal of the second NMOS transistor provides the transmission switch circuit output, and a drain terminal of the first NMOS transistor is coupled to the source terminal of the second NMOS transistor.

14. The switch circuit of claim 13 further comprising a p-channel metal oxide semiconductor (PMOS) field effect transistor having a gate terminal for receiving the first control signal, a drain terminal coupled to the source terminal of the second NMOS transistor, and a source terminal coupled to the dedicated supply signal.

15. The switch circuit of claim 12 wherein the transmission switch circuit further comprises first and second p-channel metal oxide semiconductor (PMOS) field effect transistors each having a gate terminal for receiving a second control signal complementary to the first control signal, the first and second PMOS transistors being in parallel with the first and second NMOS transistors, and wherein the transmission switch circuit passes the reference voltage signal to the transmission switch circuit output in response to the first and second control signals.

16. The switch circuit of claim 15 further comprising

a first logic level shifting circuit receiving a master control signal at an input thereof, the master control signal having a logic level determined by a first supply signal, the first logic level shifting circuit further receiving the dedicated supply signal and providing the first control signal at an output thereof; and

a second logic level shifting circuit receiving the master control signal at an input thereof, the second logic level shifting circuit further receiving the input/output supply signal and providing the second control signal at an output thereof.

17. The switch circuit of claim 15 wherein a source terminal of the first NMOS transistor and a source terminal of the first PMOS transistor provide the transmission switch circuit input, a drain terminal of the second NMOS transistor and a drain terminal of the second PMOS transistor provide the transmission switch circuit output, a drain terminal of the first NMOS transistor is coupled to the source terminal of the second NMOS transistor, and a drain terminal of the first PMOS transistor is coupled to the source terminal of the second PMOS transistor.

18. The switch circuit of claim 17 further comprising:

a third PMOS transistor having a gate terminal for receiving the first control signal, a drain terminal coupled to the source terminal of the second NMOS transistor, and a source terminal coupled to the dedicated supply signal; and

a third NMOS transistor having a gate terminal for receiving the second control signal, a drain terminal coupled to the source terminal of the second PMOS transistor, and a source terminal coupled to a common supply reference.

19. The switch circuit of claim 1 wherein the output of the transmission switch circuit is coupled to one or more input buffers for one or more I/O terminals of the logic device.

20. A switch circuit for selectively providing a reference voltage to a logic device comprising:

a first logic level shifting circuit receiving a master control signal at an input thereof, the master control signal being provided by a logic core of the logic device and having a logic level determined by a core supply signal, the first logic level shifting circuit further receiving an input/output supply signal and providing a first control signal at an output thereof, the first control signal having a logic level determined by the input/output supply signal;

a second logic level shifting circuit for receiving the master control signal at an input thereof, the second logic level shifting circuit further receiving a dedicated supply signal and providing a second control signal at an output thereof, the second control signal having a logic level determined by the dedicated supply signal, the second control signal being complementary to the first control signal, and the dedicated supply signal being different from the input/output supply signal;

a transmission switch circuit having an input for receiving the reference voltage signal, the transmission switch circuit passing the reference voltage signal to an output thereof in response to the first and second control signals.

21. The switch circuit of claim 20 wherein the logic device is operable in accordance with a plurality of input/output standards each having a specified input/output supply signal level, wherein at least one of the plurality of input/output standards is a voltage-referenced standard, and wherein the dedicated supply signal has a voltage level greater

than the lowest specified input/output supply signal level for any voltage-referenced standard.

22. The switch circuit of claim 20 wherein the dedicated supply signal has a voltage level of about 2.5 V or greater.

23. The switch circuit of claim 20 wherein the transmission switch circuit comprises

a first set of transistors comprising one or more transistors of a first type, each having a control terminal for receiving the first control signal; and

a second set of transistors comprising one or more transistors of a second type, each having a control terminal for receiving the second control signal, the first set of transistors and the second set of transistors being in parallel with one another.

24. The switch circuit of claim 23 further comprising:

a pull-down transistor coupled between a transistor in the first set of transistors and a common supply reference, the pull-down transistor being of the second type and having a control terminal for receiving the first control signal; and

a pull-up transistor coupled between a transistor in the second set of transistors and a dedicated supply signal node, the pull-up transistor being of the first type and having a control terminal for receiving the second control signal.

25. The switch circuit of claim 23 wherein

each transistor in the first set is a p-channel metal oxide semiconductor (PMOS) field effect transistor having a gate terminal for receiving the first control signal; and each transistor in the second set is an n-channel metal oxide semiconductor (NMOS) field effect transistor having a gate terminal for receiving the second control signal.

26. The switch circuit of claim 25 further comprising:

a pull-down NMOS transistor having a gate terminal for receiving the first control signal, a drain terminal coupled to the source terminal of a PMOS transistor in the first set of transistors, and a source terminal coupled to a common supply reference; and

a pull-up PMOS transistor having a gate terminal for receiving the second control signal, a drain terminal coupled to the source terminal of an NMOS transistor in the second set of transistors, and a source terminal coupled to the dedicated supply signal.

27. The switch circuit of claim 20 wherein

the first logic level shifting circuit comprises first and second n-channel metal oxide semiconductor (NMOS) field effect transistors and first and second p-channel metal oxide semiconductor (PMOS) field effect transistors, wherein the first and second NMOS transistors each has a source terminal coupled to a common supply reference, the first and second PMOS transistors each has a source terminal coupled to the input/output supply signal, the first NMOS transistor has a drain terminal coupled to a drain terminal of the first PMOS transistor and a gate terminal of the second PMOS transistor, the second NMOS transistor has a drain terminal coupled to a drain terminal of the second PMOS transistor and a gate terminal of the first PMOS transistor, and the first and second NMOS transistors have gate terminals that receive complementary versions of the control signal; and

the second logic level shifting circuit comprises first and second n-channel metal oxide semiconductor (NMOS) field effect transistors and first and second p-channel metal oxide semiconductor (PMOS) field effect transistors, wherein the first and second NMOS transistors each has a source terminal coupled to a common supply reference, the first and second PMOS transistors each has a source terminal coupled to the dedicated supply signal, the first NMOS transistor has a drain terminal coupled to a drain terminal of the first PMOS transistor and a gate terminal of the second PMOS transistor, the second NMOS transistor has a drain terminal coupled to a drain terminal of the second PMOS transistor and a gate terminal of the first PMOS transistor, and the first and second NMOS transistors have gate terminals that receive complementary versions of the control signal.

28. The switch circuit of claim 20 wherein the output of the transmission switch circuit is coupled to one or more input buffers for one or more I/O terminals of the logic device.

29. A method for selectively providing a reference voltage to a logic device comprising:

supplying a dedicated supply signal to the logic device, the dedicated supply signal being different from an input/output supply signal for the logic device;

providing a first control signal having a logic level determined by the dedicated supply signal; and

passing the reference voltage signal from a transmission switch input to a transmission switch output in response to the first control signal.

30. The method of claim 29 further comprising logic level shifting a master control signal having a logic level determined by a first supply signal to provide the first control signal.

31. The method of claim 30 further comprising generating the master control signal in a logic core of the logic device, and wherein the first supply signal is a core supply signal.

32. The method of claim 30 further comprising logic level shifting the master control signal to provide a second control signal having a logic level determined by the input/output supply signal, and wherein passing the reference voltage signal comprises passing the reference voltage signal in response to the first and second control signals.

33. The method of claim 29 wherein the logic device is operable in accordance with a plurality of input/output standards each having a specified input/output supply signal level, wherein at least one of the plurality of input/output standards is a voltage-referenced standard, and wherein the dedicated supply signal has a voltage level greater than the lowest specified input/output supply signal level for any voltage-referenced standard.

34. The method of claim 29 wherein the dedicated supply signal has a voltage level of about 2.5 V or greater.

35. The method of claim 29 further comprising:

providing protection against voltage under shoot at the transmission switch input when the voltage reference signal is not being passed to the transmission switch output; and

providing protection against voltage over shoot at the transmission switch input when the voltage reference signal is not being passed to the transmission switch output.

36. The method of claim 29 further comprising providing the reference voltage, when passed from the transmission switch input to the transmission switch output, to one or more input buffers for one or more I/O terminals of the logic device.

37. The method of claim 29 further comprising shorting a node for providing the dedicated supply signal to the input/output supply signal, when the reference voltage is not being passed from the transmission switch input to the transmission switch output.